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Comparative Analysis of Asymmetrical Multilevel Inverter Topologies

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Abstract: In this paper a comparative analysis of Asymmetrical 7-level inverter topologies suitable for photovoltaic system is offered. The analysis is done on the base of cost, components, control strategy and efficiency. Various topologies for comparative study are:(i) Conventional Asymmetrical Cascaded H-bridge topology-1(ii) H-bridge with AMLI topology-2 (iii) H-bridge with AMLI topology-3 and (iv) Boost AMLI topology-4.These topologies are used in medium as well as high voltage application. The comparative analysis investigated for the asymmetrical multilevel inverter topologies suitable for the photovoltaic system. The comparative analysis is verified via simulation study of each topology using MATLAB/ Simulink. Also the proposed topology is implemented in a prototype. The switching signals are generated using micro controller SST89E516RD.

Keywords: Multilevel Inverter (MLI), Photovoltaic (PV), cascaded H-bridge(CHB), Asymmetrical Multilevel Inverter (AMLI).

I. INTRODUCTION

Limited availability of non renewable energy sources and high power demand lead us to renewable energy source [1]. Solar energy is most popular and promising renewable energy source because using PV cell it directly converts into electrical energy. PV power is effectively utilized when the grid connected system is used. In grid connected photovoltaic system, inverter is utilized to convert the dc power produced by PV into ac feeding into the grid [2].

Generally, voltage source inverter (VSI) and current source inverter (CSI) are widely used for grid integration of renewable energy source. Nowadays, trend goes towards the utilization of multilevel inverter (MLI) because of their several benefits. MLI generates output having less alteration, produces less stress, reduces electromagnetic interference and generates better value output. It is easy to maintain and modify MLI topology as it has property of modularity. MLI also relates to lesser switching losses and smaller filter size [3] is best suited for PV applications as they are based on a series connection of several single-phase inverters. Due to this modularity, they are highly consistent.

Also, the need of different battery supplies can be fulfilled by PV modules that are available in separate form. The CHB structure is capable to reach medium output voltage levels using only standard and low voltage rating components. This topology uses least number of components.
Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage [3]. There are two type of multilevel inverter: Symmetrical MLI and Asymmetrical MLI. In symmetrical multilevel inverter each H- cell is fed by equal voltage and hence produces similar output voltage steps.

If all the cells are not fed by equal voltage, the inverters become an asymmetrical MLI. In this inverter the arm cells have different effect on the output voltage [4].The asymmetrical multilevel inverter is promising inverter topology for high voltage and high power application. This inverter synthesis several different levels of DC voltage to produce a staircase that approaches a pure sine wave. It has good power quality waveform, lower harmonic alteration, lower voltage rating of device, lower switching frequency and switching losses drop of dv/dt stresses, better efficiency.

Various topologies include multiple DC sources with semiconductor switches and H-bridge. Different valued sources, semiconductor switches and H-bridge gives seven level output.

The various AMLI topologies based on modified conventional cascaded H-bridge topology suitable for PV system. The four seven level asymmetrical inverter topologies used for comparative analysis are: (i) Conventional Asymmetrical Cascaded H-bridge topology-1 [4]. (ii)H-bridge with AMLI topology-2 [6] (iii) H-bridge with AMLI topology-3 [7] and (iv) Boost AMLI topology-4. [8]

The organization of paper is in this way: The introduction is given in section-I. Section-II describes various AMLI topologies with their structures and control strategies along with the simulation results. Section III provides the relative analysis of various topologies simulated in section-II. Section IV provides the prototype implementation of boost AMLI topology. All the simulations are executed in MATLAB/Simulink. Finally, concluding remarks are given in section-V and references are enlisted in section-VI.

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II. DIFFERENT ASYMMETRICAL MLI TOPOLOGY WITH CONTROL SCHEME AND SIMULATION

A. Conventional Asymmetrical cascaded H-bridge Topology-1

Single-phase topology of an asymmetrical cascade multilevel inverter is shown in Fig. 1. The number of output voltage levels can be raised by choosing different DC input voltage to the H-bridge without increasing no. of H-bridge cell. Thus more no. of output voltage levels can be obtained with the same H-bridge cells. An output phase voltage waveform of a cascade inverter with isolated DC voltage sources is achieved by adding the output voltages of bridges.

The DC voltage sources of all H-bridge cells are different, with the maximum number of levels of phase voltage. The asymmetrical cascade H-bridge converter consists of power conversion cells, each cell supplied by a separate DC supply on the DC side and series connected on the AC side. The two main components of the power losses in a switch are conduction losses and switching losses [4].

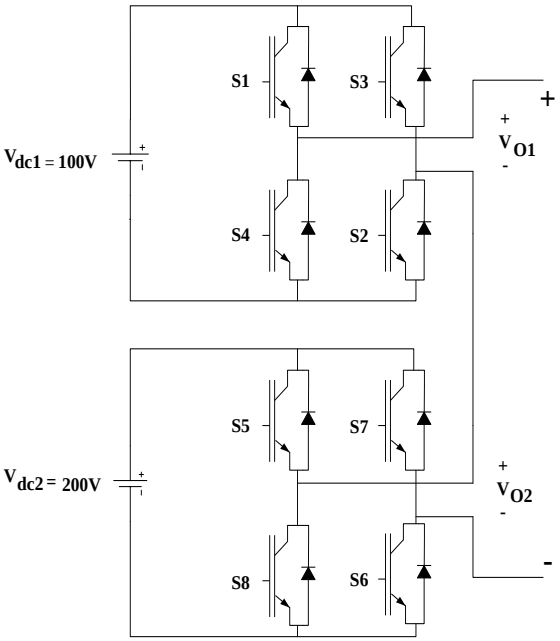

Figure 1. Cascaded 7-Level Asymmetrical MLI

Switching Sequence: To obtain different seven levels all eight switches need to operate in particular manner. When switches S1, S2 and S5, S6 are on Vo1=100V and Vo2=200V and the output voltage V=Vo1+Vo2 =300V can be obtained. When S3, S4 and S7, S8 are on output voltage V = -300V is obtained. Similarly other levels can be obtained.

The load taken is resistive load. It is described in following Table I.

TABLE I. SWITCHING SEQUENCE OF CASCADED H-BRIDGE AMLI

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Vdc1+Vdc 2	1	1	0	0	1	1	0	0
Vdc2	1	0	1	0	1	1	0	0
Vdc1	1	1	0	0	1	0	1	0
0	1	0	1	0	1	0	1	0
-Vdc1	0	0	1	1	0	1	0	1
-Vdc2	0	1	0	1	0	0	1	1
-(Vdc1+Vdc2)	0	0	1	1	0	0	1	1

The cascaded H-bridge topology is controlled using level shifted, in phase deposition multicarrier PWM switching technique[5] as shown in Fig. 2,where triangular carrier wave frequency=1000Hz and power frequency=50 Hz. The corresponding switching signals are shown in Figure 3 and the seven-level output voltage of this topology is shown in Fig. 4.

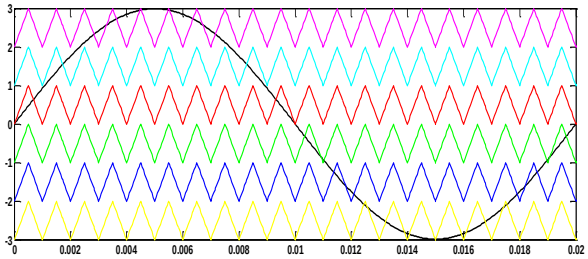

Figure 2. Level shifted, in phase deposition multicarrier modulation technique for 7-level ACHB inverter

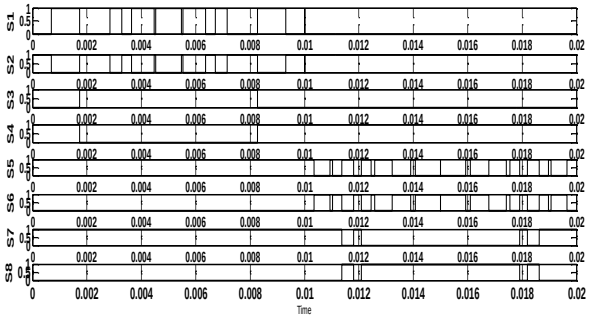

Figure 3. Switching signals for 7-level ACHB Inverter

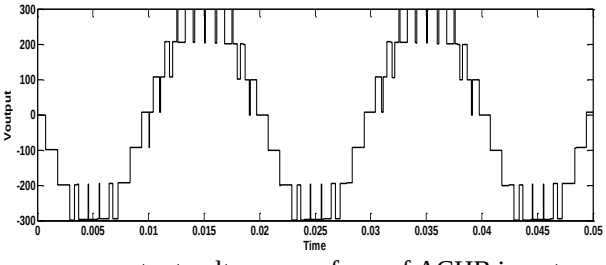

Figure 4. output voltage waveform of ACHB inverter

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B H-BRIDGE WITH MLI TOPOLOGY-2

Schematic diagram of this topology is shown in Fig. 5. As can be seen, it requires ten switches and three isolated DC supplies. The main idea of this topology as a multilevel inverter is its left portion in Fig. 5.It generates the required output levels. This part requires the switches having high frequency. The bridge circuit chooses the polarity of the output voltage. It can be known as polarity generation. It requires the switches having low frequency. It can be used for three-phase applications with the same basic.

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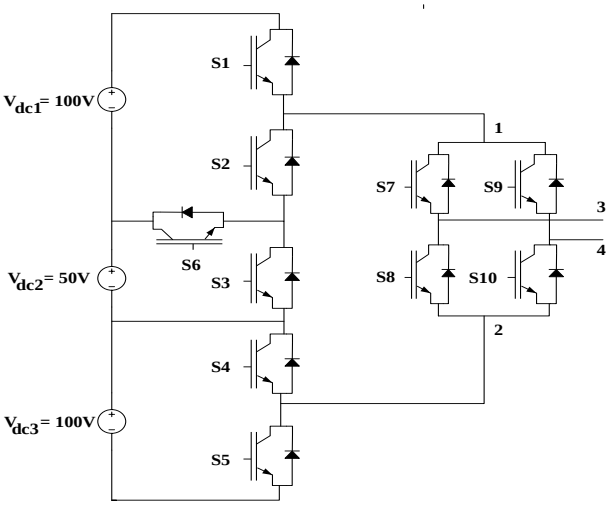

Figure 5. H-bridge with AMLI topology-2

Switching sequence: To obtain different seven levels, all the ten switches need to operate in particular manner. It is described in following Table II.

TABLE II SWITCHING SEQUENCE OF H-BRIDGE WITH AMLI TOPOLOGY-2

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
Vdc1+Vdc2+Vdc3	1	0	0	0	1	0	1	0	0	1
Vdc2+Vdc3	0	1	0	0	0	1	1	0	0	1
Vdc2	0	1	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	1	0	0	1
- Vdc2	0	1	0	1	0	1	0	1	1	0
-(Vdc2+Vdc3)	0	1	0	0	0	1	0	1	1	0
-(Vdc1+Vdc2+Vdc3)	1	0	0	0	1	0	0	1	1	0

The multiple source topology is simulated according to operation of the topology described in Table 2 and the load taken is resistive load. To control this MLI topology same multicarrier PWM technique as in Figure 2,where triangular carrier wave frequency=1000Hz and power frequency=50Hz is used and the resulting switching signals given to each switch are shown in Fig. 6 and obtained seven level output voltage is shown in Fig. 7.

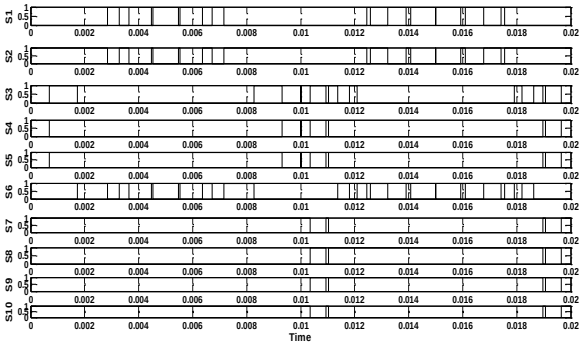

Figure 6. Switching signals for H-bridge with AMLI topology-2

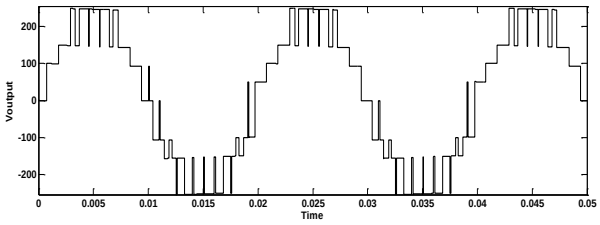

Figure 7. output of H-bridge with AMLI topology-2

C.H-bridge with AMLI topology-3

Fig. 8 shows a configuration of the single phase 7-level inverter having One H- Bridge, four switches and two isolated DC sources. It consists of an H-Bridge module and two level modules, consisting of components S5, S6, Vdc2 and S7, S8, Vdc1.

To obtain the voltage levels, proper switches in H-Bridge and Level Modules are activated at the correct angle values. Thus 7- level output voltage levels (0,±Vd, ±2Vd and ±3Vd) are obtained by using proper battery voltages (Vd, 2Vd, Vd+2Vd). According to switch position, the output voltage levels are shown in Table III.

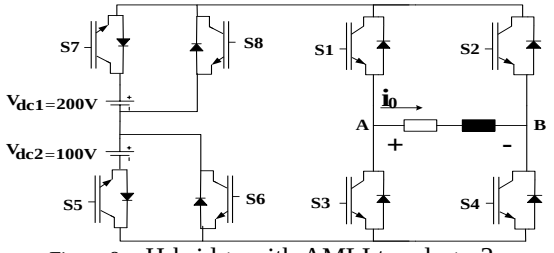

Figure 8. H-bridge with AMLI topology-3

Switching sequence: To obtain different seven levels, all eight switches need to operate in specific manner. It is described in following Table III. The all operational

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states(±Vd, ±2Vd and ±3Vd) and free whiling state(0level) are shown in Table III. The switch S8 and S6 are in on state only in regenerating state means when output current is zero.

This AMLI topology is simulated according to operation of the topology described in Table 3, using control scheme multicarrier PWM technique as in Fig. 2,where triangular carrier wave frequency=1000Hz and power frequency=50Hz and the load taken is resistive load. The resulting switching signals are shown in Fig. 9. And seven level voltage output is shown in Fig. 10.

Thus this AMLI topology can be operated in three states: Operating state, Freewheeling state and Regenerating state.

TABLE III. SWITCHING SEQUENCE OF H-BRIDGE WITH AMLI TOPOLOGY-3

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Vdc1+ Vdc2	1	0	0	1	1	0	1	0
Vdc1	1	0	0	1	0	0	1	0
Vdc2	1	0	0	1	1	0	0	0
0	1	1	0	0	0	0	0	0
-Vdc2	0	1	1	0	1	0	0	0
-Vdc1	0	1	1	0	0	0	1	0
-(Vdc1 +Vdc2)	0	1	1	0	1	0	1	0

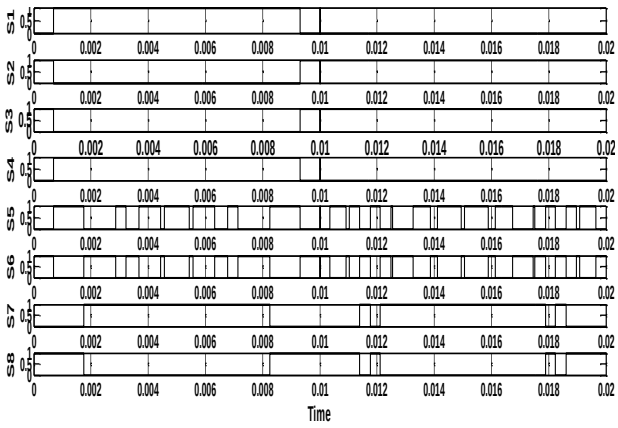

Figure 9. Switching signals for H-bridge with AMLI topology-3

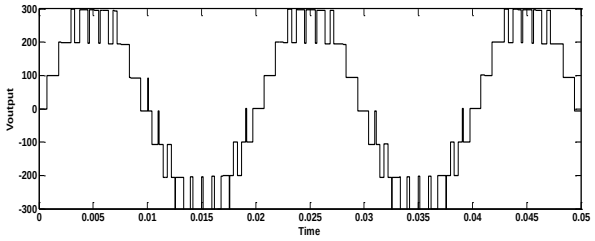

Figure 10. Output of H-bridge with AMLI topology-3

D. AMLI topology-4

The asymmetrical one seven level inverter with single input DC source is shown in Fig. 11. The Boost converter is used to produce an asymmetrical DC link voltage of Vdc and 2Vdc across capacitors C1 and C2. It consists of an inductor L, diodes D1, D2, IGBT switch S5 and capacitors C1, C2 on the boost side. S1, S2, S3, S4 and S5 are the switches for switched capacitors where as S6, S7, S8 and S9 are the switches of H- bridge cell. To verify simulation result with developed prototype the input DC supply voltage is taken 12V and the load taken is resistive load.

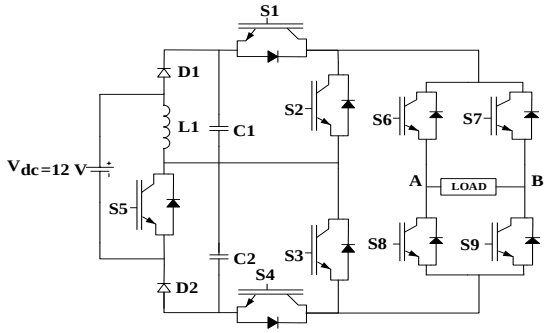

Figure 11. Boost AMLI topology-4

Mode 1[VO=0V]: Switches S6 and S7 are turned ON to produce zero voltage at the output. Both capacitances C1 and C2 remain unchanged during this mode.

Mode 2[VO=1Vdc]: Switches D1, S1, S3 and S5 are operated and the input voltage is connected across the inductor L and capacitor C1. In this way capacitor C1 charges Vdc. At the same time, switches S6 and S9 are turned ON to produce Vdc at the output.

Mode 3[VO=2Vdc]: Switches S3, S6, S9, S4 and D2 are turned ON at the same time to charge the capacitor C2 to 2Vdc. since the inductor (L) boosts the source voltage from Vdc to 2Vdc when the duty cycle is 50%.

Mode 4[VO=3Vdc]: To obtain 3Vdc output level at the inverter, a discharge path is provided by turning ON the auxiliary switches S1 and S4 with H-bridge switches S6 and S9.

Mode 5-7: The switching operation of MOB converter and auxiliary switches to produce -Vdc, -2Vdc and -3Vdc are similar for the modes 5-7 as like mode 2, 3 &4. But the H-bridge cell complementary switches on the same leg S7 and S8 is operated instead of S6 and S9 switches. The complete operation of charging and discharging of capacitors of above discussed modes for a single cycle is given in Table IV [8].

Switching sequence: To obtain different seven levels, all nine switches need to operate in specific manner.It is described in following Table IV.

Fig. 12 shows the generalized proposed control scheme. It consists of three stages with the following features: In stage 1, reference and carrier signals are enabled to required modulation signal. The carrier signals higher than the reference of desired sine wave frequency give 1 or else 0. Similarly carrier signals are compared above the time axis Cx and below the time axis Cy to generate the control pulse for positive and negative half cycles. In stage 2,

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manipulations are carried out with the control pulses to generate the aggregated signals fagg(t) and to get the desired. In stage 3, the look up table is prepared based on the topology. The sine and carrier wave control scheme are shown in Fig. 13,where triangular carrier wave frequency=5000Hz and power frequency=50 Hz. The switching signals are generated as shown in Fig. 14 and the seven level output voltage is generated as shown in Fig. 15.The voltage across capacitor C1 is 12v,across C2 is 24V and seven level output voltage is 34V.

TABLE 4 SWITCHING SEQUENCE OF BOOST AMLI TOPOLOGY-4

Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_8
$3V_{DC}$	1	0	0	1	0	1	0	0	1
$2V_{DC}$	0	1	0	1	0	1	0	0	1
V_{DC}	1	0	1	0	1	1	0	0	1
0	0	0	0	0	0	1	1	0	0
$-V_{DC}$	1	0	1	0	1	0	1	1	0
$-2V_{DC}$	0	1	0	1	0	0	1	1	1
$-3V_{DC}$	1	0	0	1	0	0	1	1	0

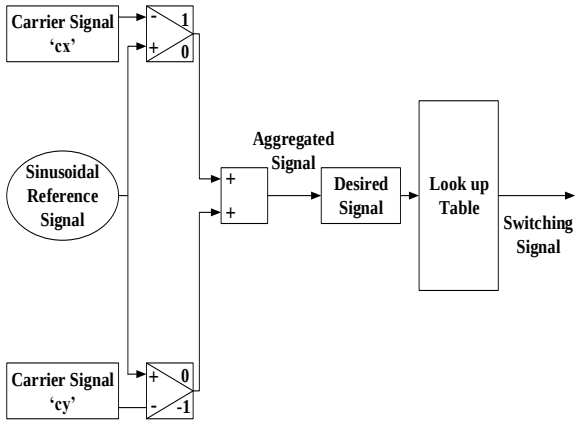

Figure 12. Generalized block diagram of control system

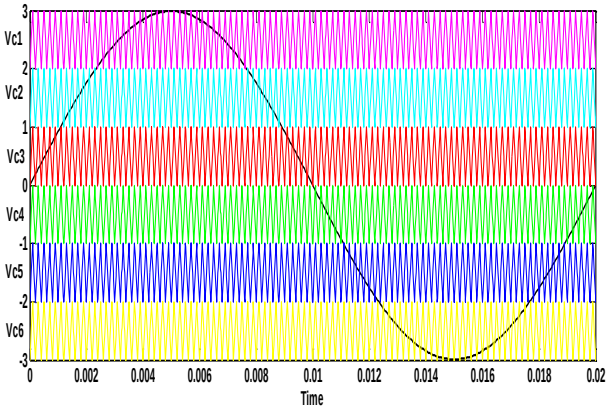

Figure 13: Triangular and Sine Wave modulation technique for Boost AMLI

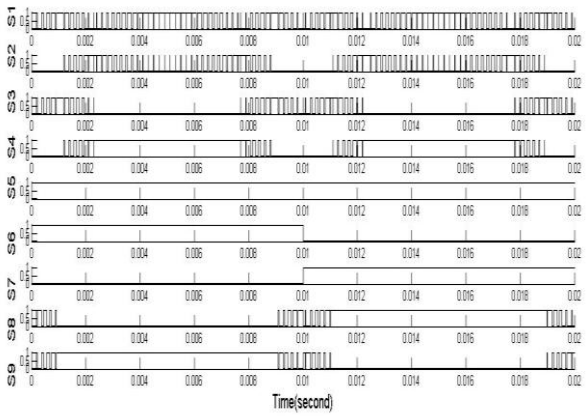

Figure 14: Switching signal of 7-level boost AMLI topology

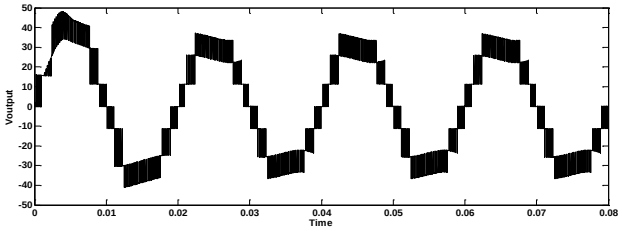

Figure 15: Output voltage of Boost AMLI topology

III. COMPARISON OF DIFFERENT TOPOLOGIES FOR SEVEN LEVEL

The comparison of the four different seven-level asymmetrical inverter topologies is described in this section in light of components used and photovoltaic application.

Conventional cascaded H-bridge topology (Fig. 1) requires two single phase H-bridges. The numbers of levels in the output phase voltage can be varied by changing the value of source voltage of any H-bridge. These source voltages are PV modules output voltage. The numbers of components required are large but have an advantage of identical modular structure. It is suitable for stand-alone PV system.

H-bridge with MLI topology-2 (Fig. 5) requires only one H-bridge, ten switches, three sources and seven levels can be achieved. This topology has superior feature over conventional topology in terms of the modularity, control and reliability. Number of output voltage levels can be increased just by adding two switches and one DC source. If all three sources are having the same value it may be symmetrical MLI.

H-bridge with MLI topology-3 (Fig. 8) requires only one H-bridge, four switches, two sources and seven levels can be obtained. In this topology most important feature of the system is being convenient for expanding and increasing the number of output levels simply by adding cascaded level module..It can increase the number of output levels with a four switching devices.

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Boost AMLI topology (Fig. 11) requires only one H-bridge, no of switches are nine, one source, one inductor, two diodes and two capacitors. This topology requires comparatively less components among all. So the cost of the overall structure is relatively less. Also, it uses only one source. Therefore, large PV array with single MPP tracker can be used. The control involves less number of carriers compared to other topology. Also it has one additional feature of boosting in output voltage. Although there is a problem of voltage balancing amongst the capacitors, it can be improved by additional component and proper switching. This can be used for standalone system as well as it is the best suited inverter topology for grid connected photovoltaic system.

The brief summary of comparative analysis of four different seven-level inverter topologies suitable for PV system is given in Table V based on number of components, number of dc sources etc. Based on this analysis boost AMLI topology is selected for prototype.

TABLE: 5 COMPARITIVE ANALYSIS OF AMLI TOPOLOGIES FOR 7-LEVELS

	AMLI Topology 1	**AMLI Topology 2**	**AMLI Topology 3**	**AMLI Topology 4**
No. of switches	8	10	8	9
Dc bus capacitor	0	0	0	2
No. of Sources	2	3	2	1
H-Bridge Cell	2	1	1	1
Boosting Voltage Capacity	No	No	No	Yes

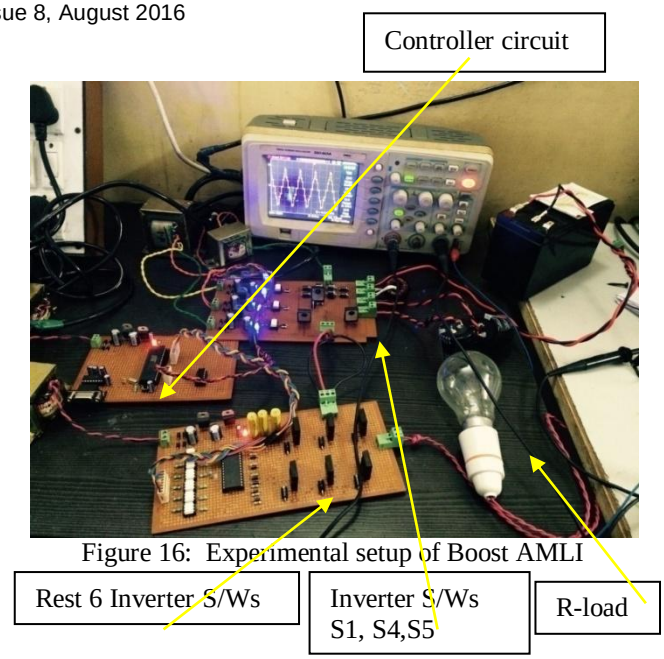

Figure 16: Experimental setup of Boost AMLI

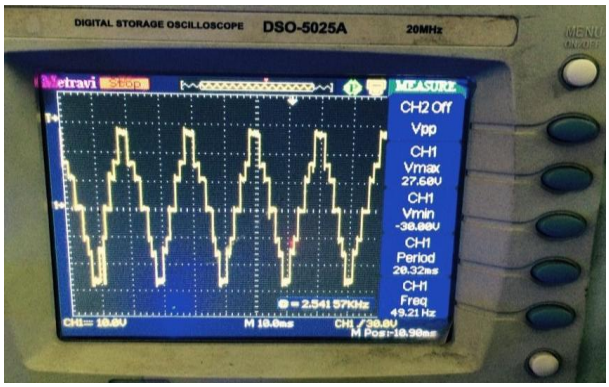

Figure 17 seven level output of designed prototype (Voutput=29V,50Hz)

IV. EXPERIMENTAL RESULTS

Fig. 16 shows the experimental setup for boost AMLI topology-4. As shown in this figure main three modules are used,

i) Inverter Circuit
ii) Micro Controller (**SST89E516RD)**
iii) MOSFET Driver Circuit

Supply voltage in AMLI prototype is taken DC 12V, capacitors C1=C2=470µF, inductor L=1mH. The switches (S1 to S9) in AMLI are MOSFET IRF P450.In microcontroller SST89E516RD all nine switching signals (as shown in Fig.14) are generated. To drive the switches S2,S3,S6,S7,S8 and S9 driver IR2130 is used. To drive the switches S1, S4 and S5 isolated driver TLP250 is used. As a resistive load incandesce lamp of 100W rating is used.

The prototype demonstrates the voltage across capacitors C1 is 11V and across C2 is 18V. Fig. 17 is the seven level output voltage of asymmetrical boost topology. It is peak to peak 29 V.

V. CONCLUSION

In this paper different types of asymmetrical MLI topology for seven level output voltage are studied. A new topology front end boost asymmetrical seven level inverter with single DC input source is presented with its typical control scheme. This converter maintains the specified DC link voltage with the objective of boosting the input voltage as well as level generator for the inverter operation. The H-bridge part produces voltage levels polarities at the output. This topology is having voltage boosting capacity, less number of components, less cost and easy control scheme for PV system compared to conventional topologies. Thus this topology is selected to develop a prototype. For the same given DC input voltage, nearly same output voltage levels and voltage magnitude with the prototype is obtained as obtained in simulation.

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